Advanced Space Systems for Users #2
(Structured Information Systems)

UPN 310-90-18

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Semi-Annual Review of the FY97 SOMO/MO&DSD Technology Development Program

April 15, 1997

Structured Information Systems

High Performance Data Compression

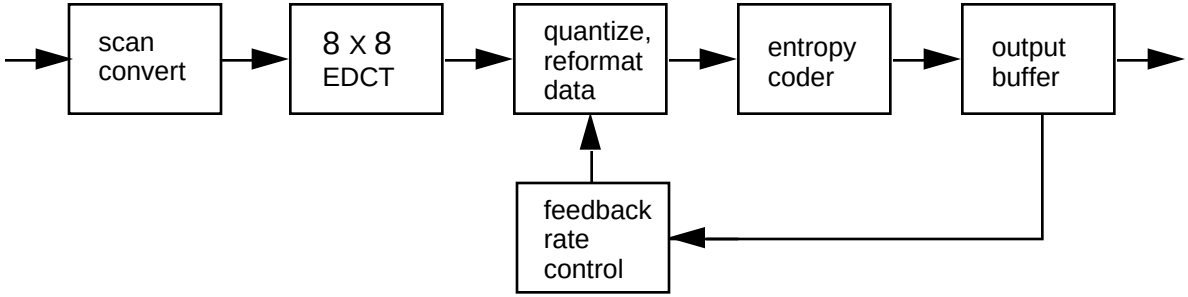
GSFC

- **Background**
  - **Determined HPDC requirements by surveying potential users and consideringspace environment constraints.**
  - **Developed algorithm based on requirements and previously designed entropyencoder space flight Integrated Circuit (IC).**
  - **Simulated HPDC Technology on different imaging science applications andcompared to other algorithms.**
  - **Algorithm baselined for SSTI/Lewis mission for HSI and LEISA instruments.**
- **Accomplishments**
  - **Entropy Decoder ASIC layout is completed, no testing errors, AMI 0.6 micron technology selected as foundry.**
  - **HPDC preprocessor ASIC performs 4 kinds of calculations: Forward and Inverse, Enhanced Discrete Cosine transform (EDCT), as well as DCT with up to 16 bits per sample at 25 Msps.**
  - **Developed two algorithms for the HPDC, DCT spectral component processor which are currently being studied by GSFC, the University of New Mexico, and Aerospace Corporation.**
  - **Completed SSTI/Lewis (TRW) pre flight end-to-end HPDC tests.**

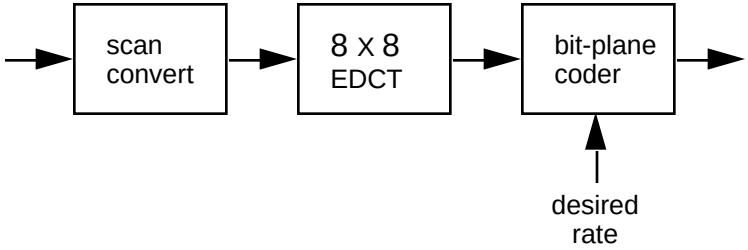
- Complete design and fabricate entropy decoder ASIC.
- Complete design FY97, fabricate HPDC/EDCT ASIC FY98.
- Adaptive Quantizer/Bit Plane ASIC Specification FY97.
- SSTI/Lewis Launch May 1997 with Hyper Spectral Imager HPDC Experiment.

Enhanced DCT System

Scheme 1



Scheme 2



Advantage over JPEG system:

- No need to design and load Huffman coding tables for various quantization and applications (scheme 1 and 2)
- Better image quality at the same bit rate (scheme 1 and 2)
- Better and easier control of desirable output bit rate (scheme 2)

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High Rate Channel Coding

- Background
  - Determine the state-of-the-art of present commercially available Viterbi decoder.
  - University of Hawaii (UH) investigated complexities of various sectionalized Trellis diagram for the RM (64,40) code and discovered a specific 8-Trellis structure which will minimize decoding complexity and will have the potential to achieve a decoding speed of 600 Mbps.
  - University of Notre Dame determined Turbo Code theory and verified its performance.

Accomplishments

- **Accomplishments**

600 Mbps Viterbi Decoder:

- Design of the Add-Compare-Select Unit (ACSU) is completed and currently being verified using a C-Code behavioral mode.
- The ACSU prototype ASIC will be fabricated by LSI logic using the .65 micron CMOS processes.
- Completed architecture for 300 Mbps decoder using 0.6 micron CMOS process which is a pipelining of three ASIC: Branch Metric Unit, ACSU, and an Arbitrator Unit (600 Mbps will require two decoders operating in an interleaving manner).

TCM/Turbo Code:

- Investigated performance of using an outer (255,239) Reed-Solomon Code concatenated with a rate 1/2 Turbo Code.

Papers Published:

- "Good Non-Minimal Trellises for Linear Block Codes", IEEE Transaction on Communication, 1/97.
- "Multidimensional Trellis Coded Phase Modulation Using a Multilevel Concatenated Approach", IEEE Transaction on Communication, 1/97.

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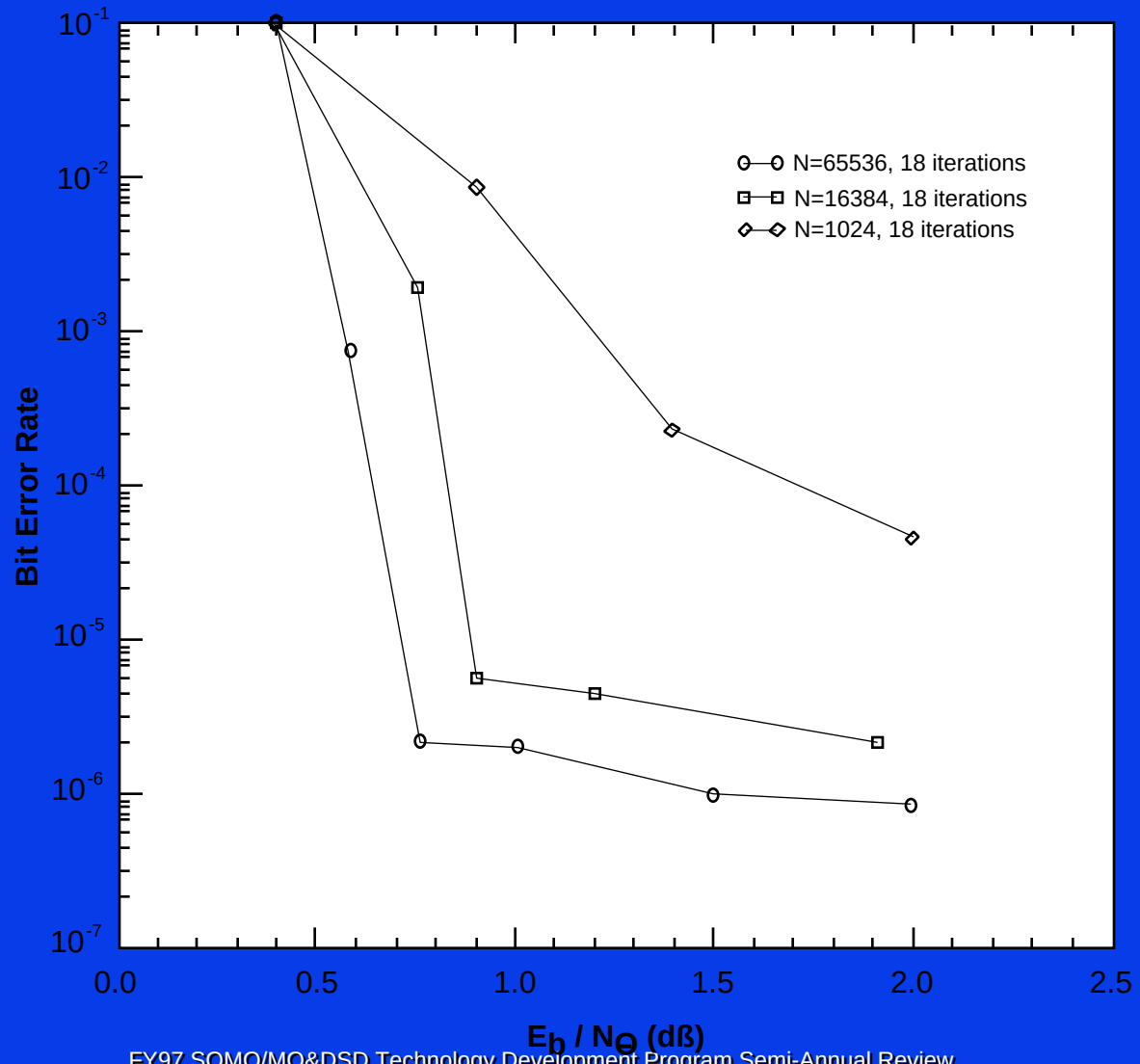
Performance of Turbo Codes

GSFC



High Rate Channel Coding (FY97 Goals)

- Fabricate and evaluate the prototype ACSU for the RM (64.40) subcode.
- Continue to research the error pattern distribution of the Turbo Code and its impact on the outer coding technique.